a die having a high power supply voltage node and a low power supply voltage node; and

a transistor coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

10. [Amended] The circuit of claim 9, wherein the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and the drain are coupled to the low power supply voltage node.

14. [Amended] A circuit comprising:

a die;

a ground node located on the die;

a power supply voltage node located on the die; and

an electronic device permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node.

16. [Amended] The circuit of claim 14, wherein the [bias] operational node voltage is about 1.3 volts.

REMARKS

Applicant has reviewed and considered the Office Action mailed on July 12, 2001 and the references cited therewith.

Claims 4, 9, 10, 14, and 16 are amended, no claims are canceled, and no claims are added; as a result, claims 4-6, 9, 10, and 14-16 are now pending in the application.

Objections to the Specification

The specification was objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 C.F.R. 1.75(d)(1) and MPEP § 608.01(o). The Office Action

asserts that the operating voltage of "between about .5 volts and about 1.5 volts" in claim 5 lacks an antecedent basis. Applicant traverses the objection.

37 C.F.R. 1.75(d)(1) requires that "the meaning of the terms in the claims" be ascertainable by reference to the description. Applicant respectfully submits that 37 C.F.R. 1.75(d)(1) does not require claim terms that are clear on their face to be repeated in the remainder of the specification. The terms objected to -- "between about .5 volts and about 1.5 volts" -- are clear on their face, so repeating these terms in the remainder of the specification is not required.

For the reasons stated, applicant requests withdrawal of the objection to the specification.

Rejections Under 35 U.S.C.§112

Claims 4-6 and 14-16 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant traverses the rejection.

The specification, at page 5, lines 1-14, recites the following:

> Voltage variable capacitors are capable of *decreasing* noise signals of one polarity and *increasing* noise signals of the opposite polarity. A metal oxide semiconductor field effect transistor (MOSFET), fabricated and configured in the embodiments described below, is one type of active device that exhibits this property and can be applied to a variety of signal processing applications.
>
> Referring to Figure 1C, data point 103 shows that for an inversion mode capacitor having a noise value of about $^{-}$.10, the depletion mode capacitor has a noise value of less than $^{-}$.10. So, the MOSFET operating in the depletion mode and having a voltage variable capacitance characteristic is capable of reducing the noise level below the noise level for a MOSFET operating in the inversion mode having a fixed value capacitor. (emphasis added)

Applicant notes that the above description also includes the asymmetrical limitation objected to. The reason for this is that "an inversion mode capacitor having a noise value of about $^{-}$.10, the depletion mode capacitor has a noise value of less than $^{-}$.10" are asymmetrical.

Applicant respectfully submits that the above quoted description enables claims 4-6 and claims 14-16.

Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 4-6 and claims 14-16.

Claims 4-6 and 14-16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Office Action rejects claim 4 and asserts that the phrase "the operating voltage value. \" is not grammatically correct. Claim 4 is amended to correct the typographical error. Claim 4 is not amended in response to an art rejection.

The Office Action rejects claim 4 and asserts that the transistor recited is not connected to other claim elements. Claim 4 is amended to clarify the connection of the transistor to other claim elements. Claim 4 is not amended in response to an art rejection.

The Office Action rejects claim 4 and asserts that "... capable of ..." does not positively recite a circuit function and that it is not clear whether the claimed function occurs. Applicant traverses the rejection.

Applicant respectfully submits that functional language is specifically authorized by *In re Swinehart*, 439 F.2d210, 169 USPQ 226 (CCPA 1971); MPEP § 2173.05(g). For the purpose of determining indefiniteness claims are read in light of the specification. The scope of claim 4, when read in light of the text at page 5, lines 10-14 (provided above), is clearly not indefinite.

Thus, for the amendments and reasons stated above, claim 4, as amended, is not indefinite.

Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 4.

Claims 5-6 are dependent on claim 4. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that claims 5-6 are not indefinite. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 5-6.

The Office Action rejects claim 14 and asserts that the language of claim 14 is indefinite in that the function claimed may not occur. Applicant traverses the rejection.

For the purpose of determining indefiniteness claims are read in light of the specification. The scope of claim 14, when read in light of the text at page 5, lines 10-14 (provided above), is clearly not indefinite.

Thus, for the amendments and reasons stated above, claim 14, as amended, is not indefinite.

The Office Action rejects claim 14 and asserts that the recited electronic device is not connected. Applicant traverses the rejection.

The electronic device is intended to be connected as claimed, which is in such a way that "an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node" are provided by the connection.

Thus, claim 14 is not indefinite.

Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 14.

Claims 15-16 are dependent on claim 14. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that claims 15-16 are not indefinite. Furthermore, claim 16 is amended to correct the antecedent basis problem noted in the office action.

Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims15-16.

Rejections Under 35 U.S.C.§102

Claims 9-10 and 14-16 were rejected under 35 U.S.C.§102(e) as being anticipated by Sin (U.S. Patent No. 5,130,564).

Claim 9, as amended, recites "... a transistor coupled between the high power supply voltage node and the low power supply voltage node ... ."

In contrast, Sin in FIG. 5A shows a variable capacitor (VCL) coupled between voltage nodes V_0 and V_R. However, since V_{CC} and V_{SS} represent "the high power supply voltage node" and "the low power supply voltage node," respectively, in FIG. 5A, Sin does not show the VCL coupled between "the high power supply voltage node" and "the low power supply voltage

node." In addition, even when transistor PM switches on, only one node N of the VCL is coupled to "the high power supply voltage node." The other node is coupled to a ground node.

Hence, since the VCL is not coupled between "the high power supply voltage node" and "the low power supply voltage node," Sin does not teach a "... a transistor coupled between the high power supply voltage node and the low power supply voltage node ..." as recited in claim 9.

Thus, since Sin does not teach each of the elements recited in claim 9, the Office Action fails to state a *prima facie* case of anticipation with respect to claim 9. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 9.

Claim 10 is dependent on claim 9. For reasons analogous to those stated above and the elements in the claim, applicant respectfully submits that claim 10 is not anticipated by Sin. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 10.

Claim 14, as amended, recites "... an electronic device permanently coupled between the ground node and the power supply voltage node ... ."

In contrast, Sin in FIG. 2A shows a capacitive load (CL) coupled between a node common to transistors PM and NM and a ground node. FIG. 2A also shows the CL as switchable between the node common to the transistors PM and NM and power supply voltage node V_{CC}.

Hence, since the CL is not is not permanently coupled between the ground node and V_{CC}, Sin does not disclose "... an electronic device permanently coupled between the ground node and the power supply voltage node ..." as recited in claim 14.

Thus, since Sin does not teach each of the elements recited in claim 14, the Office Action fails to state a *prima facie* case of anticipation with respect to claim 14. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 14.

Claims 15-16 are dependent on claim 14. For reasons analogous to those stated above and the elements in the claim, applicant respectfully submits that claims 15-16 are not anticipated by Sin. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claims 15-16.

So called "prior art" "made of record but not relied upon"

Several patents were cited as "pertinent to applicant's disclosure" but not relied upon to reject claims. In view of the fact that the patents were not asserted against any claims, applicant need not respond either to the assertion of their pertinence or to the assertion that any of the listed patents constitutes "prior art" to any pending claim. Applicant expressly reserves the right to challenge any such assertion, should it be included in some future rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone applicant's attorney at 612-371-2109 to facilitate prosecution of the application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

RAJENDRAN NAIR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2109

Date January 11, 2002 By Danny Padys

Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 11 day of January, 2002.

Jane E. Brockschink
Name

Jane E. Brockschink
Signature